quioxane (HSQ) or methyl silsesquioxane (MSQ). An annealing may be performed to cure the material of STI regions **120**, and liner **118** may prevent (or at least reduce) the diffusion of semiconductor material from fins **116** (e.g., Si and/or Ge) into the surrounding STI regions **120** during the annealing. Other processes and materials may be used. A chemical mechanical polish (CMP) or etch back process may be used to level a top surface of the dielectric material of STI regions **120** using pad layer **110** (e.g., a nitride) as an etch stop layer. After planarization, top surfaces of fins **116** and STI regions **120** may be substantially level with each other. Furthermore, in embodiments where semiconductor layer **106** is tensilely strained, n-type anti-punch through (APT) impurities (e.g., boron or BF_2) may be implanted in semiconductor layer **106**.

As further illustrated by FIG. **6**, a barrier layer **122** may be formed over STI regions **120** and fins **116**. In various embodiments, barrier layer **122** may be blanket deposited using any suitable process (e.g., CVD, and the like). Barrier layer **122** may act as a mask layer, an etch stop layer, and/or a protective layer for various underlying features during the formation of additional features in wafer **100** as will be explained in greater detail in subsequent paragraphs. In some embodiments, barrier layer **122** may comprise a different material than pad layer **110**, which may allow for selective patterning of barrier layer **122** or pad layer **110**. For example, when pad layer **110** comprises a nitride, barrier layer **122** may comprise an oxide (e.g., SiO, ALD OX, plasma enhanced oxide (PEOX)). In some embodiments, barrier layer **122** may have a thickness of about 15 nm to about 30 nm, for example.

FIGS. **7** through **10** illustrate the removal of top portions of certain fins **116** (labeled **116'**). Referring first to FIG. **7**, barrier layer **122** is patterned using a combination of photolithography and etching, for example, to form an opening **126** extending through barrier layer **122**. The patterning of barrier layer **122** may include using photoresist **124** as a patterning mask and an anisotropic etching process. Opening **126** may partially expose a top surface of STI regions **120** and top surfaces (e.g., pad layer portions **110'**) of semiconductor fins **116'**. In such embodiments, pad layer portions **110'** may act as an etch stop layer for the etching of barrier layer **122**. The fins exposed by opening **126** may be one selected for the formation of finFETs of a different type (e.g., p-type) than n-type semiconductor strips **106**. In alternative embodiments where semiconductor layer **106** is a p-type layer, n-type finFETs may be formed in fins **116'**. Other fins **116** in wafer **100** may remained masked by barrier layer **122**. Subsequently, photoresist **124** may be removed using a photoresist stripping solution, such as, "Caro's Solution" or "Caro's PR Solution," for example.

Next, in FIG. **8**, pad layer portions **110'** (e.g., a nitride) of fins **116'** are removed using one or more etching processes, for example. The removal of pad layer portions **110'** may include a dry etching process to break through a native oxide (not shown) formed on a top surface of exposed STI regions **120** followed by a dry etching to remove pad layer portions **110'**. The removal of pad layer portions **110'** may further use pad layer portions **108'** (e.g., an oxide) as an etch stop layer.

As a result of break through etching, a top surface of STI regions **120** in opening **126** may be recessed by a distance D**1** from a top surface of masked portions of STI regions **120**. For example, barrier layer **122** may prevent damage to masked portions of STI regions **120** and fins **116** during the break through etching process. In various embodiments, the break through etching process may use a chemical etchant that selectively etches STI regions **120** at a higher rate than barrier layer **122**. For example, a ratio of the etching rate of barrier layer **122** to the etching rate of STI regions **120** may be about 1:1.5. In such embodiments, barrier layer **122** may also be etched during the break through etching (not explicitly illustrated).

Referring next to FIG. **9**, pad layer portions **108'** and n-type semiconductor strips **106'** of fins **116'** are removed using one or more etching processes, for example. The removal of pad layer portions **108'** (e.g., an oxide) may include a break through etching process, and subsequently, a channel recess (e.g., a dry or wet etching process) may be employed to remove n-type semiconductor strips **106'**. The removal of pad layer portions **108'** may comprise a similar process as the break through etching used to remove the native oxide (not shown) of exposed STI regions **120**. In such embodiments, distance D**1** may be increased during the removal of pad layer portions **108'**, and embodiments, barrier layer **122** may prevent damage to masked portions of STI regions **120** and fins **116** during the removal of pad layer portions **108'**. The removal of pad layer portions **108'** and n-type semiconductor strips **106'** may further recess portions of liner **118** exposed by opening **126** (e.g., by a distance D**2** in FIG. **9**). In some embodiments (not illustrated), liner **118** may even be recessed past a top surface of SRB layer **104**. Subsequently, an ashing process may be used to clean out byproducts of the etching processes (e.g., break through etching and/or channel recessing). Thus, trenches **128** are formed in wafer **100** disposed between neighboring STI regions **120**. Trenches **128** may be connected to opening **126** and expose top surfaces of SRB layer **104** in fins **116'**.

In FIG. **10**, an epitaxial pre-cleaning is performed to remove a native oxide (not shown) formed on a top surface of SRB layer **104** in trenches **128**. The pre-cleaning process may include using an HF-based gas or a SiCoNi-based gas, for example. As a result of pre-cleaning, a top surface of STI regions **120** in opening **126** may be recessed even further from a top surface of masked portions of STI regions **120** (e.g., D**1** may be further increased).

As also illustrated by FIG. **10**, liner **118** may substantially cover sidewalls of trenches **128**. For example, top surfaces of liner **118** and STI regions **120** may be substantially level after the pre-cleaning process. Alternatively, liner **118** may be recessed from the top surface of SRB layer **104**. In subsequent process steps (e.g., in FIG. **11**), semiconductor strips **130** may be grown in trenches **128** on SRB layer **104**. In embodiments where liner **118** is recessed, semiconductor strips **130** may be grown on multiple surfaces of SRB layer **104** (e.g., a lateral top surface and sidewall surfaces). This increased bonding area may reduce the occurrence of voids and other interface defects at the interface between SRB layer **104** and semiconductor strips **130**.

Throughout the various etching and/or pre-cleaning processes illustrated by FIGS. **8** through **10**, barrier layer **122** may prevent damage to masked portions of STI regions **120** and fins **116**. As a result of various etching/pre-cleaning processes, barrier layer **122** may also be thinned. Thus, the deposition of barrier layer **122** may include depositing a sufficiently thick layer to withstand these various process steps. For example, barrier layer **122** may have an initial thickness (after deposition) of about 15 nm to about 30 nm.

After pre-cleaning, in FIG. **11**, an epitaxy is performed to epitaxially grow semiconductor strips **130** are formed in trenches **128**. In various embodiments, semiconductor strips **130** may be of a different type than n-type semiconductor strips **106**. For example, in wafer **100**, semiconductor strips **130** may be p-type layer, and will be referred to as p-type semiconductor strips **130** hereinafter. Various embodiments